REMARKS

Claims 1-6 were pending in the present application. By virtue of this response, claims 1, 3, and 4 have been amended. Claim 2 has been cancelled. Accordingly, claims 1 and 3-6 are currently under consideration. Amendment and cancellation of certain claims is not to be construed as a dedication to the public of any of the subject matter of the claims as previously presented. Claim 1 is amended to correct the lack of antecedent basis of the term "common word line" where recited for the first time in the claim. In addition, claim 1 is amended to include the subject matter of claim 2. Claim 3, previously dependent from claim 2, is amended to depend from claim 1. Claim 4 is amended to correct the lack of antecedent basis of the terms "common word line" and "common bit line" where recited for the first time in the claim. No new matter has been added.

Rejections under 35 U.S.C. §102(e)

The Office has rejected claims 1-3 under 35 U.S.C. § 102(e) as allegedly being anticipated by Yamada (6,822,895) ("'895 patent"). Applicants respectfully traverse.

As an initial matter, Applicants respectfully submit that no filing date, domestic or foreign, of the '895 patent was before November 29, 2000, contrary to the statement made by the Examiner in ¶ 5 of the Office Action. Therefore, the changes made to § 102(e) in 1999 and 2002 do apply when considering this reference as prior art. MPEP 2136.03.

Claim 1 has been amended to include the limitations recited in claim 2. Applicants respectfully submit that the rejection under § 102(e) with respect to amended claim 1 should be withdrawn because the '895 patent does not disclose each and every claim limitation recited in amended claim 1.

Amended claim 1 recites a memory device including a variable resistive element whose electrical resistance is changed due to an electrical stress. The '895 patent does not disclose or suggest the variable resistive element recited in claim 1. As stated in the Specification of the present application, the resistance of the variable resistive element changes in response to voltage

pulses. Specification at pages 3-4. With respect to original claim 2, the Examiner has stated that "Yamada ['895 patent] discloses wherein the variable resistive element is a variable resistive element whose electrical resistances are changed due to an electrical stress (Column 7, lines 32-41)..." Office Action at page 4. Applicants respectfully disagree. The passage cited by the Examiner in the '895 patent (col. 7, lines 32-41) discloses only variable resistive elements that are "storage element[s] exhibiting ferromagnetic resistance," specifically TMR (tunneling magnetoresistance) elements. TMR elements have two ferromagnetic layers separated by an insulating nonmagnetic layer. '895 patent, col. 7, lines 25-31. For the resistance of the TMR element to be changed, the alignment of the ferromagnetic layers is changed from parallel to antiparallel or vice versa by exposure to current creating sufficiently high magnetic field. '895 patent, col. 1, lines 44-57. Thus, the '895 patent does not disclose or suggest the variable resistive element that changes resistance in response to an electrical pulse recited in amended claim 1.

Since amended claim 3 depends from amended claim 1, and amended claim 1 is not anticipated by the '895 patent, Applicants submit that the rejection under § 102(e) for claim 3 should be withdrawn.

In addition, the Office has rejected claims 1-6 under 35 U.S.C. §102(e) as allegedly being anticipated by Yamada (6,760,244) ("'244 patent"). Applicants respectfully traverse.

In response, Applicants respectfully submit that the '244 patent does not qualify as prior art under § 102(e). No application date, domestic or foreign, for the '244 patent was before November 29, 2000. Therefore, the changes to § 102(e) instituted in 1999 and 2002 apply to consideration of this reference as prior art. MPEP 2136.03. The foreign priority date under § 119 (a)-(d), (f) or § 365(a) of a reference not be used as the critical date for § 102(e) purposes. MPEP 2136.03 (citing In re Hilmer, 359 F.2d 859 (CCPA 1966)). Applicants submit that the critical date of the '244 patent for § 102(e) purposes is its U.S. filing date of January 29, 2003. Furthermore, Applicants submit that they are entitled to the benefit of the foreign priority date under § 119 for the present application of December 5, 2002. MPEP 2136.03. Since Applicants' priority date predates

the critical date of the '244 patent, Applicants submit that the rejection under § 102(e) should be withdrawn.

Furthermore, even if Applicants are not entitled to the benefit of their foreign priority date, Applicants respectfully submit that the '244 patent does not disclose each and every limitation of amended claim 1 and therefore the rejection under § 102(e) should be withdrawn.

The '244 patent does not disclose or suggest the memory device including a variable resistive element whose electrical resistance is changed in response to an electrical stress recited in amended claim 1. The Examiner has stated that the '244 patent discloses a variable resistive element whose resistance electrical resistances are changed due to an electrical stress at column 1, lines 25-65. Office Action at pages 4-5. Applicants respectfully disagree. The passage cited by the Examiner ('244 patent, col. 1, lines 25-65) does not disclose or suggest the variable resistive element recited in amended claim 1. Instead, the cited passage discloses only storage elements comprising two ferromagnetic layers with a non-magnetic layer between the ferromagnetic layers, specifically GMR (giant magnetoresistance) and TMR (tunneling magnetoresistance) elements. TMR and GMR elements change resistance in response to a magnetic field which causes the magnetizations in the two ferromagnetic layers to be either parallel or antiparallel to each other. '244 patent, col. 1, lines 44-60. Thus, the '244 patent does not disclose or suggest a variable resistance element whose resistance is changed in response to an electrical stress as recited in amended claim 1.

Since amended claim 3 depends from amended claim 1, and amended claim 1 is not anticipated by the '244 patent, Applicants submit that the rejection under § 102(e) for claim 3 should be withdrawn.

With respect to claim 4, even if Applicants are not entitled to the benefit of their foreign priority date, Applicants respectfully submit that the '244 patent does not disclose each and every limitation of claim 4 and therefore the rejection under § 102(e) should be withdrawn.

Claim 4 recites memory cells having one end of a variable resistive element connected to the source of a first selection transistor and the other end of the variable resistive element connected to the drain of a second selection transistor, wherein the drain of the first transistor is connected to a common bit line and the source of the second selection transistor is connected to a source line.

The '244 patent discloses a memory device having a completely different architecture than that recited in claim 4. The memory device of the '244 patent includes a memory cell formed from two TMR cells and two selection transistors. The '244 patent does not disclose the limitation that the source of a second selection transistor is connected to a source line. Although there is a second transistor (5b) in the memory cell in Fig. 1 of the '244 patent, it is not analogous to the second selection transistor of claim 4. The source/drain of the second transistor 5b of the '244 patent is connected to an inverted bit line (/BL), not to a source line. The inverted bit line of the '244 patent is not equivalent or analogous to the source line of the present application. In the '244 patent, the signal level on the inverted bit line changes in a complementary manner with the signal level on the bit line. (col. 7, lines 28-31). In contrast, the source line of the present application is independent from the bit line.

The '244 patent also does not disclose the limitation recited in claim 4 that the variable resistive element is connected on one end to the source of a first selection transistor and on the other end to the drain of a second selection transistor. In the '244 patent, the drain of one selection transistor is connected to a bit line (BL) and the drain of the other selection transistor is connected to an inverted bit line (/BL). Following the Examiner's references to Fig. 1 of the '244 patent, first variable resistive element 4a is connected on one side to the source/drain of a transistor 5a, but the other end of first variable resistive element 4a is connected to one end of a second variable resistive element 4b, not to the drain of a second transistor.

Thus, the '244 patent does not disclose or suggest the memory device recited in claim 4.

Claims 5 and 6 ultimately depend from claim 4, and since claim 4 is not anticipated by the '244 patent, Applicants submit that the rejection under § 102(e) for claims 5 and 6 should be withdrawn.

CONCLUSION

In view of the above, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to withdraw the outstanding rejection of the claims and to pass this application to issue. If it is determined that a telephone conference would expedite the prosecution of this application, the Examiner is invited to telephone the undersigned at the number given below.

In the event the U.S. Patent and Trademark office determines that an extension and/or other relief is required, applicant petitions for any required relief including extensions of time and authorizes the Commissioner to charge the cost of such petitions and/or other fees due in connection with the filing of this document to Deposit Account No. 03-1952 referencing docket no. 559502000600. However, the Commissioner is not authorized to charge the cost of the issue fee to the Deposit Account.

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Respectfully submitted,

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